Syllabus – ELEC 427 (Fall 2014)

- Title: "Advanced Digital Hardware Design, Implementation, and Optimization"
  - CRN 12070

- Instructor / TA
  - Prof. Farinaz Koushanfar, farinaz@rice.edu
  - Teaching assistant: Ebrahim Songhori, em24@rice.edu

- Meeting time
  - 09:25AM - 10:40AM TR

- Office hours
  - After lecture or by appointment; TA session Wed 4-5pm

- Prerequisites
  - Assuming undergraduate level knowledge of logic design, 326 or Equivalent

- Reading
  - Lecture notes
  - Recommended books
  - Papers and tutorials

- Class webpage
  - Owlspace: https://owlspace-ccm.rice.edu/
  - Check for updates, syllabus, lecture notes, labs, assignments, etc.

- Description: The course's objective is development of the necessary skills to design simple processors suitable for numerically intensive tasks; emphasis on FPGA implementation flow. We consider the system-level and block-level design of digital signal processing (DSP) algorithms. We shall review logic design and implementation of control and data flow functions. The students would learn the Verilog hardware description language for implementing the function. The course covers high-level DSP optimizations such as pipelining, unfolding, and parallel processing. Memory and architecture level techniques are also discussed. Common DSP algorithms such as FFTs, finite impulse response (FIR) filters, and matching algorithms are covered. The course has a strong practical component. The students learn modeling of DSP algorithms in Matlab and conversion of Matlab models into Verilog blocks. System implementation on FPGA boards, optimization and verification are required for the final project.

- Recommended books (not required, the lectures are self-contained):
  - David Money Harris and Sarah L. Harris, Digital Design and Computer Architecture, Second Edition © 2012 by Elsevier Inc.

  - Pong P. Chu, FPGA Prototyping by Verilog Examples: Xilinx Spartan-3 Version, ISBN-978-0-470-18532-2, Wiley-and Sons, 2008.
  - Digital Design an Embedded Systems Approach Using VERILOG, Peter J. Ashenden, ISBN: 978-0-12-369527-7, Morgan Kaufmann, 2008.
  - VLSI Digital Signal Processing Systems: Design and Implementation, Keshab K. Parhi, ISBN: 978-0471241867, Wiley, 1999.
  - The Design Warrior's Guide to FPGAs, Devices, Tools and Flows, Clive "Max" Maxfield, Newnes Publishers, ISBN: 0750676043, 2004.
  - Digital Signal Processing with Field Programmable Gate Arrays, Uwe Meyer-Baese, ISBN: 978-3540726128, 3rd Edition, Springer, 2007.
  - Verilog references will be available on the course webpage

- Grading
  - Lab assignments (25%), Mid-term (20%), Final (10%), Class project report (30%), Class project presentation (10%), Participation (5%)

- Project: Groups of 2 or 3 (collaborations encouraged)

- Tentative course outline
  - Week 1: Orientation and overview of FPGAs, review of number presentation, sequential and combinational circuits
  - Week 2: Combinational logic blocks
  - Week 3: Sequential logic blocks
  - Week 4: FPGA design flow
  - Week 5: Finite State Machines in Verilog
  - Week 6: FPGA optimization and comparison
  - Week 7: Floating point algorithms, memory, and clock issues on FPGAs and Implementation examples, e.g., FIR, ciphers, etc.
  - Week 8: In-class mid-term after fall recess, introduction of the final project at a system level ,
  - Week 9: Testing and evaluation of FSMs
  - Week 10: Practical implementations methods
  - Week 11: FIR filters
  - Week 12: IIR Filters
  - Week 13: FFT block
  - Week 14: Systematic design optimization for power, area, timing
  - Week 15: Final project presentation and reports (Report)